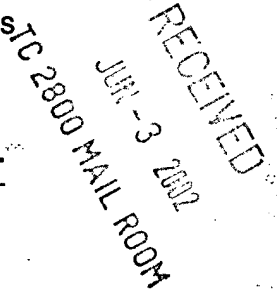
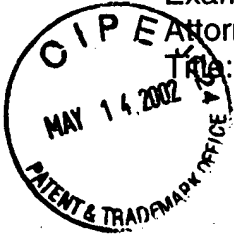


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/332,271
Filing Date June 11, 1999
Inventor Klaus Florian Schuegraf et al.
Assignee Micron Technology, Inc.
Group Art Unit 2812
Examiner Ron E. Pompey
Attorney's Docket No. MI22-532
Title: Methods for Forming Wordlines, Transistor Gates, and Conductive Interconnects,
and Wordline, Transistor Gate, and Conductive Interconnect Structures



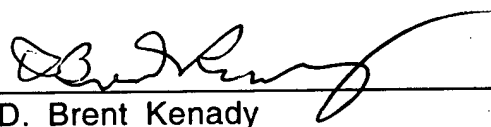
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

References -- See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56. No admission is made regarding whether any of the submitted references is prior art. Copies of the references are attached.

Respectfully Submitted:

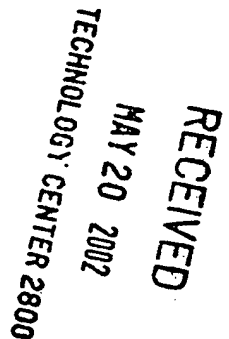
Dated: 5-6-02


D. Brent Kenady
Reg. No. 40,045

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PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
MI22-532SERIAL NO.
09/332,271LIST OF ART CITED BY APPLICANT
(Use several sheets if necessary)APPLICANT
Klaus Florian SchuegrafFILING DATE
June 11, 1999GROUP
2812

U.S. PATENT DOCUMENTS

Examiner Initials		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,472,896	12/95	Chen et al.	437	44	
	AB	5,393,685	02/95	Yoo et al.	437	44	
	AC	4,833,099	05/89	Woo	437	41	
	AD	5,915,197	06/99	Yamanaka et al.	438	586	
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
	AM							
	AN							
	AO							
	AP							
	AQ							

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AR		
	AS		
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EXAMINER

DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered.
Include copy of this form with next communication to applicant.